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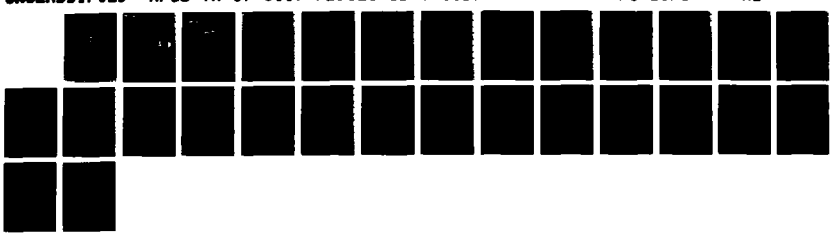

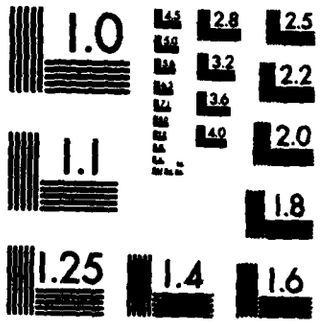

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PROGRAMMABLE PCM ENCODER

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"This Technical Report has been reviewed and is approved for publication"

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FOR THE COMMANDER

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This paper will present the concept of a general purpose pulse code modulation (PCM) encoding system which has all the major operating parameters under stored program control. This type of encoder can be used in a large variety of scientific/engineering data gathering applications by simply programming an onboard EPROM to tailor the encoder to the specific mission requirements. Key Words: Pulse Code Modulation (PCM), Encoder, Data Acquisition, Parity, Programmable Filter, Multiplexer.

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PROGRAMMABLE PCM ENCODER

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INTRODUCTION

The modulation methods for the transmission of data from sounding rockets and high altitude balloons has gradually progressed from FM/FM to almost exclusively pulse code modulation (PMC) over the last 20 years. This is due in part to the more flexible formatting, increased overall accuracy capability and efficient transmission and recording of the PCM signals. As a direct consequence of this flexibility in formatting, a particular PCM encoding system can be closely matched to specific experimental requirements to give the desired accuracy, frequency response, and number of channels while still conserving transmission bandwidth.

The PCM encoder system presented in this paper provides a method of selecting the operational parameters by stored program without any hardware changes.

OVERVIEW

PCM encoders, in general, have many operating parameters which must be specified to meet the requirements of a particular application. These include number and types of inputs, sampling rate of each input, accuracy of encoding, parity requirements, type of output code, type of synchronization codes, bit rates, and output filter requirements. Often the requirement of a particular application will change as the mission becomes better defined. This results in a decision to either specify a new encoder or relax the requirements to allow the existing encoder to be used.

A study was initiated to lead to the development of an encoder which would incorporate a single microcomputer chip and be software controlled. It was felt that with such an encoder it would merely be necessary to write the necessary program for storage in an EPROM in order to adapt to the changing requirements of an individual program. Furthermore, as new missions with changed requirements arose, the same basic encoder could be used without the need to redesign or modify the hard wired logic.

The resulting encoder can accept a number of analog and digital signals and multiplex them into a serial digital data stream for subsequent transmission. It is totally controlled by an on board single component 8-bit microcomputer. By programming the memory (an EPROM

contained within the microcomputer), all the operating parameters can be set to meet a specific application. This program memory is large enough to contain several completely different formats which could, if so desired, be changed by activating a single interrupt line. This feature would allow format changes in flight. This programming feature also allows complete changes in format at any point in a program by simply inserting a new preprogrammed microcomputer into the encoder or reprogramming the existing one. A block diagram of the entire system is shown in Figure 1. and a complete schematic drawing is available.

The following is a tabulation of the various parameters available to the user:

Analog Inputs - Up to 158 analog inputs can be serviced with full scale input levels from 78 mV to 10 volts. Each channel can have different full scale input levels and the channels can be selected in any order. The analog channel frequency response is limited only by the rate at which a particular channel is sampled. For differential input capability, up to 8 different signal returns may be selected.

Digital Inputs - Up to 64 direct digital entry channels are available. Each channel may contain up to 12 bits per word. All digital channels are connected to a single 12 bit bus and the user must present his data through a tristate

gate which is enabled by the encoder. The encoder will accept signals which are compatible with low power Schottky TTL levels.

Word Length and Parity - Word length from 8 to 132 bits plus a parity bit can be accommodated. Parity can be even or odd and is located in the MSB position if used.

Bit Rate - The bit rate can be programmed from 2 bits/sec. to 700 k bits/sec. All bit rates are digitally synthesized from a single crystal controlled oscillator.

Output Code - The following codes are available. NRZ-L, NRZ-M, NRZ-S, BiO-L, BiO-M, BiO-S, DM-M and DM-S. (See Reference 1. for definition of codes.)

Premodulation Filter - The output filter is a 6 pole (36 dB/octave rolloff) linear phase low pass active filter with a 3 dB cutoff range of 640 Hz to 700 kHz.

Output Signals - Besides the PCM output, two output synchronization clocks are available. They are a PCM bit rate and word rate clocks. Also outputted are the signals to synchronize the entry of the direct digital entry signals. Address lines are also outputted and can be decoded for synchronization purposes (major frame sync., minor frame sync.) or a particular data word.

Frame Formats - Any channel may be supercommutated and any channel may be subcommutated. The maximum number of minor frames to major frames is 256. The major frame synchronization may be accomplished by either ID mode,

pattern mode or complimentary frame sync. mode. Maximum word rate is 61.1 kilowords per second and is limited by the microcomputer cycle time.

Physical - Electrical - Power required for the encoder is approximately +15 V at 96 mA, -15 V at 96 mA, and -5 V at 750 mA. The physical dimensions are 8.5 x 5.75 x 3 inches or 21.59 x 14.61 x 7.62 cm and weights 3.25 lbs. or 1.48 kg. Flight models flown in Brazil on the BIME (Brazil Ionospheric Modification Experiment) program and those built for the SES (Sensor Ejection System) program had different aspect ratios, but approximately the same volume.

DETAILED CIRCUIT DESCRIPTION

a) Data Input Circuitry. Figure 2. is a block diagram of the data input circuits. Both analog and digital data sources may be accessed by the encoder and may be acquired in any sequence as they are under control of the program stored within the microcomputer.

Analog signals pass through a bank of analog multiplxers, which are protected to withstand input voltages exceeding the supply voltages by 10 volts and can withstand brief input transient spikes of several hundred volts. After selection, the desired signal goes to a programmable gain differential amplifier (PGDA) and is amplified such that the net result is a full scale voltage of 10 volts. The range of fullscale input voltages is from 78 millivolts

to 10 volts. The voltage range from each source can be different since the gain of the PGDA is under program control. The differential feature of the PGDA allow selection of the appropriate signal return such that ground loops and ground induced noise can be minimized.

All analog signals pass through a sample and hold circuit, and then encoded to 12 bits. The actual number of bits transmitted is under software control and is determined during the initialization routine. After encoding, the data (now in digital form) is placed on to a data bus from which it will be converted to a serial pulse train at the proper time and bit rate.

The direct digital input signals are organized such that each user inputs his signals on a common 12 bit digital input bus through a tristate gate. These gates are under control of the PCM encoder microcomputer. Gating control signals are available to the user such that data will be ready for access at the proper time. The direct digital bus passes through a buffer before it enters the data bus for serial conversion.

b) Parity Generating Circuit. Figure 3. is a functional diagram of the parity generating circuit. This circuit generates an odd or even parity bit. The most significant 7 data bits from the data bus are applied to the parity generator directly. The least significant 5 data bits are applied to the 5 AND gates. These AND gates allow

the masking of the data if the data length is less than 12 bits. The ODD/EVEN control adds an additional 1 or 0 to the parity generator to change the parity from odd to even. The parity bit is sent to the parallel to serial conversion circuit where, if selected, it is added to the serial data stream in the most significant bit position. The masking bits, odd/even control bit, and parity select bit are controlled by the byte code latched into port 7 during the initialization routine which occurs during power up.

c) Bit Rate Frequency Synthesis. A block diagram of the basic phase-locked-loop bit rate generator is shown in Figure 4. The elements of the system are a phase comparator, loop filter, a voltage controlled oscillator, and three 16-bit divide-by-N binary counters. The division ratio of each counter is set during the initialization routine. The voltage controlled oscillator, or VCO, is an oscillator whose frequency is proportional to an externally applied voltage. [When the loop is locked, the VCO frequency is exactly equal to the output of counter 0, which is derived from the TO output of the microcomputer times the division factor of counter 1 which is driven by the VCO.] The phase detector produces a dc or low-frequency signal proportional to the phase difference between the outputs of counter 0 and counter 1. This phase sensitive signal is passed through the loop filter and is applied to the control input of the VCO. The output of the VCO also

drives the input to counter 2. The output of counter is then buffered and inverted to become the bit rate clocks, PCM CK and PCM CK. The frequency generated by this process has the same long term stability as the microcomputer clock crystal.

The bit rate can be calculated from the counter division factors and the TO clock as shown below:

$$f_{PCM} = f_{TO} \times \frac{1}{N_0} \times N_1 \times \frac{1}{N_2} = \frac{f_{TO} N_1}{N_0 N_2}$$

[When the loop is locked the VCO frequency is exactly equal to N^1 times the output of counter 0, thus both inputs to the phase comparator are equal in frequency.] where

f_{PCM} = Resultant bit bate

f_{TO} = Microcomputer clock frequency (3.667 MHz)

N_0 = Division rate of counter 0

N_1 = Division rate of counter 1

N_2 = Division rate of counter 2 (Counter must be an even number for a symmetric output).

including the constraints of other circuits in the encoder, bit rates from 2 Hz to 700 kHz are possible, with a maximum frequency error of 0.015%.

d) Output Code Generation and Selection. Figure 5. is excerpted from the master drawing. It includes the logic circuits which produce all the standard IRIG PCM codes. All basic codes are continuously generated from the NRZ-L input

and the PCM clocks (0 and 0). The specific code to be outputted is selected by a digital data selector, which is controlled by the code latched into Port 9 during the initialization routine. The selected code is then routed to a six pole active filter.

e) Premodulation Filter and Output Drives. The premodulation filter, shown in abbreviated block form in Figure 6 is a 6 pole linear phase low-pass active filter. The cutoff range can be varied from 640 Hz to 700 KHz. Selection of cutoff frequency is accomplished by selecting appropriate resistors and capacitors with digitally controlled analog gates. This active filter was designed using the unity gain Sallen-Key approach.

Each of the three filter sections provides a pair of complex poles which when properly positioned yield the desired linear-phase response. Programming of the cutoff frequency is accomplished during the initialization routine with the digital result being latched into port 10, a programmable peripheral interface. This 6 bit digital word drives analog gates to the R and C block of the diagram. Preceeding the filter is a unity gain buffer, which provides isolation and DC offset adjustment. This offset adjustment is necessary because the transmitters are DC coupled and a DC component in the wave train would offset the center frequency of the radiated signal, possibly out of range of the crystal controlled receivers.

Following the active filter are two drive circuits. The first is the transmitter modulation driver. Its main function is to provide variable gain for setting of the transmitter deviation. This is accomplished by driving a potentiometer followed by a unity gain amplifier.

The second drive circuit is a video line driver which drives a 50 ohm coaxial cable from the vehicle to the blockhouse. This allows full PCM monitoring without requiring that the RF system be activated. This feature is important in areas where RF radiation clearance is limited to short periods of time due to other programs in progress on the same range.

f) Timing Circuits. The timing circuits shown in block diagram form in Figure 7. provide all essential timing functions required for proper encoder operation. A timing diagram displaying these timing functions is shown in Figure 8. and an explanation of their operation is given below.

During the initialization routine the number of bits per word is outputted to PORT 8, a programmable peripheral interface. This binary number is applied to the data inputs on a synchronous binary down counter. When this counter reaches its terminal count, its output RCO goes low for one bit period. This brings S/L low on the parallel to serial converter which permits the data on the data bus to be parallel loaded on the next leading edge of the PCM CK. RCO is also applied to a D type flip-flop where it is delayed by

one-half bit period and inverted. The Q output of this flip-flop designated T1 in Figure 1. accomplishes the following task on its lead edge: (1) it clocks out the next data bus control word which determines whether an analog, digital, or sync word is to be placed on the bus, (2) it starts a 5 microsecond delay in the A/D control, (3) and it sets the TEST 1 flip-flop which causes a program branch within the microcomputer. After the 5 microseconds has elapsed the sample control goes high which places the sample and hold circuit into the hold mode as indicated in Figure 8. One microsecond later the start conversion pulse goes low initiating an analog to digital conversion with a conversion time of 8 microseconds.

As an illustration a typical analog channel X is followed from an analog signal input to a serial digital signal out. As mentioned earlier the leading edge of T1 sets the TEST 1 flip-flop which causs a program branch within the microcomputer. The analog channel X selection code and bus control word will appear at PORT 1 of the microcomputer within 6.0 to 9.82 microseconds. The selection code is applied to the data input circuits where analog channel X and its return are selected and allowed to settle. The bus control word is applied to the bus control buffer/latch until it is clocked out by the next T1 pulse. At this time the bus control word is decoded and enables the analog data buffer placing the outputs of the A/D converter

onto the data bus. The same T1 pulse also starts a 5 microsecond delay in the A/D control circuit. This delay allows the maximum settling time in the analog circuits before going into the hold mode. One microsecond later the analog to digital conversion starts and is complete in 8 microseconds. The valid parallel data signal is placed onto the data bus through the already enabled analog data buffers. The next parallel load signal loads the data into the parallel to serial converter. Now the data is clocked out one bit at a time in NRZ-L format to the code generator.

As a second illustration, the outputting of a SYNC or ID word will be examined. Again the sequence begins with the setting of the TST 1 flip-flop. A program branch is initiated within the microcomputer and as before a bus control word appears at PORT 1. Also a SYNC or ID word is outputted to PORT 5 and PORT 6. The bus control word is applied to the bus control buffer/latch and the SYNC or ID word is applied to the frame sync. and ID buffer/latch. At the next T1 pulse the bus control word is clocked out and decoded which enables the sync. and ID buffer/latch placing this data on the data bus. The next parallel load signal loads the data into the parallel to serial converter where it is now clocked out in serial form.

APPLICATIONS

Programmable encoders developed under this Air Force contract have been successfully utilized in sounding rocket programs at Natal, Brazil, Wallops Island, Virginia and White Sands Millile Range (WSMR) in New Mexico. They are currently being employed in the Polar Ionospheric Irregularities Experiment (PIIE) scheduled for January 1985 from Greenland and the Beam Emission Rocket Technology (BERT) program scheduled for spring of 1985 from WSMR. Application in shuttle experiments are now at the proposal stage.

FUTURE DEVELOPMENT

The following areas of circuitry and packaging are now being investigated to improve performance and expand application:

1. Power Consumption - The present encoder consumes approximately 7 watts of power which in most applications presents no difficulties, but in certain long term applications this would overburden the available capacity of the system batteries. A direct replacement CMOS version of the 8748 microcomputer has become available, which along with a CMOS analog to digital converter (ADC) and the replacement of the low power Schottky logic with their equivalent CMOS logic would reduce the power consumption to

less than 0.5 watts. The CMOS ADC would result in a lower maximum bit rate, but this is not a limitation in most applications.

2. The encoders, up to the present time, have used wire wrap construction techniques. While this method of construction is reliable and allows for easy changes in circuitry, it is very labor intensive and produces a relatively high volume package. Because of these deficiencies, a printed circuit version of this encoder is being developed for future applications.

3. Several circuitry changes are under consideration which would reduce the size and/or complexity of the encoder. Incorporation of programmable logic arrays for code generation and design of a synthesized response output filter are some of these areas. Also being investigated is the possibility of using electrically erasable programmable read only memories (EEPROM) which would allow a PCM format to be changed without physically opening the package. This would have application on shuttle borne experiments where physical access to equipment is restricted long before flight.

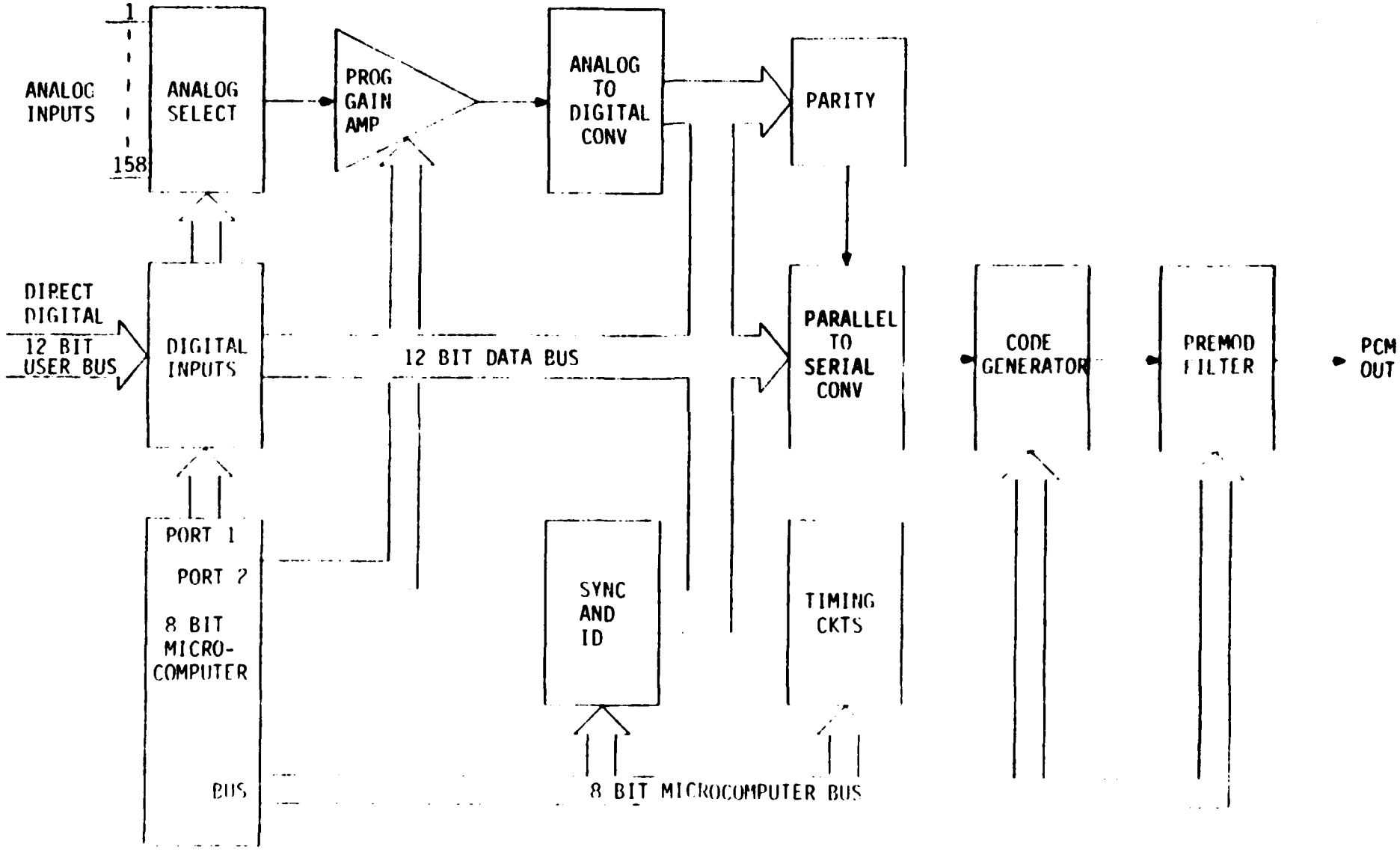

FIGURE 1. SYSTEM BLOCK DIAGRAM

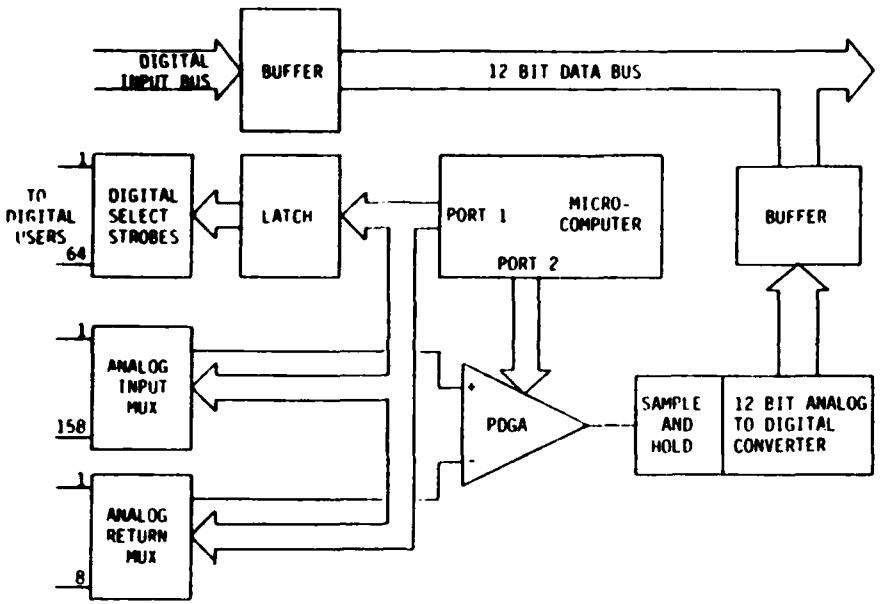

FIGURE 2. DATA INPUT CIRCUITRY

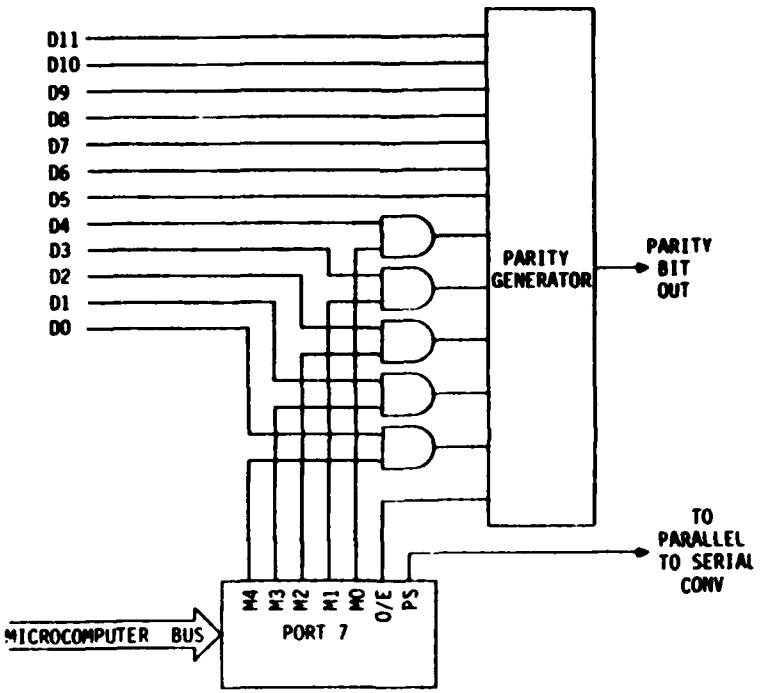

FIGURE 3. PARITY GENERATING CIRCUIT

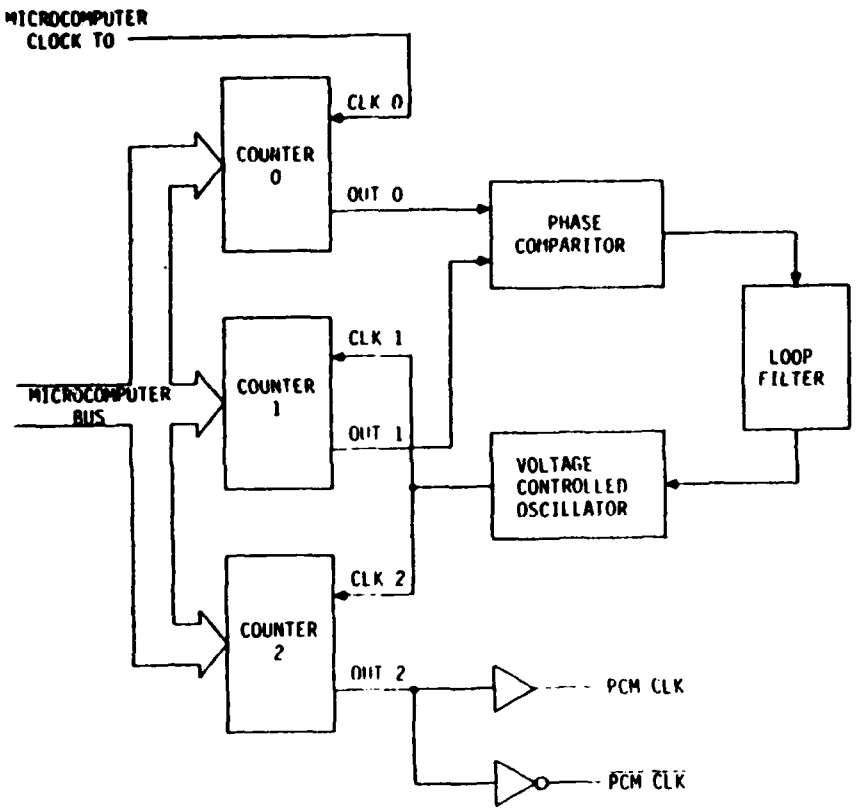

FIGURE 4. BIT RATE FREQUENCY SYNTHESIS

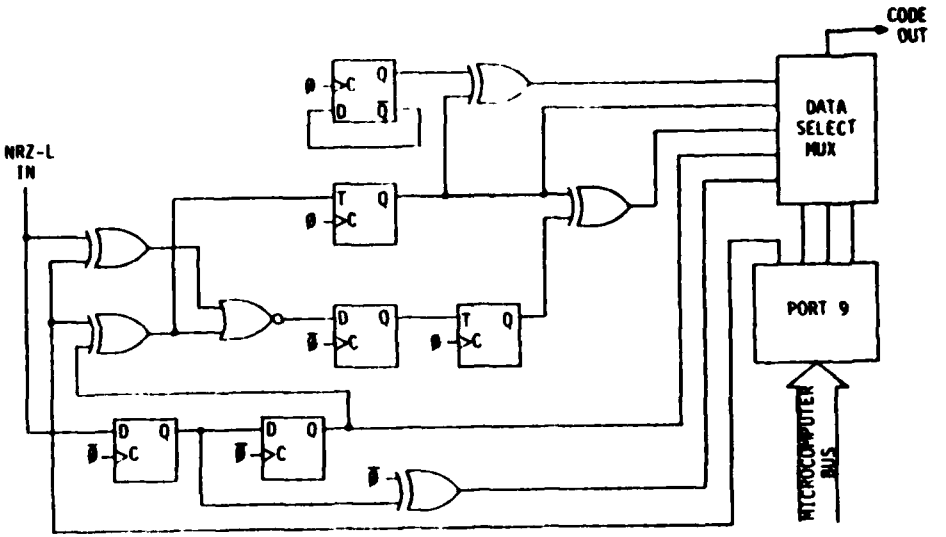

FIGURE 5. OUTPUT CODE GENERATION AND SELECTION

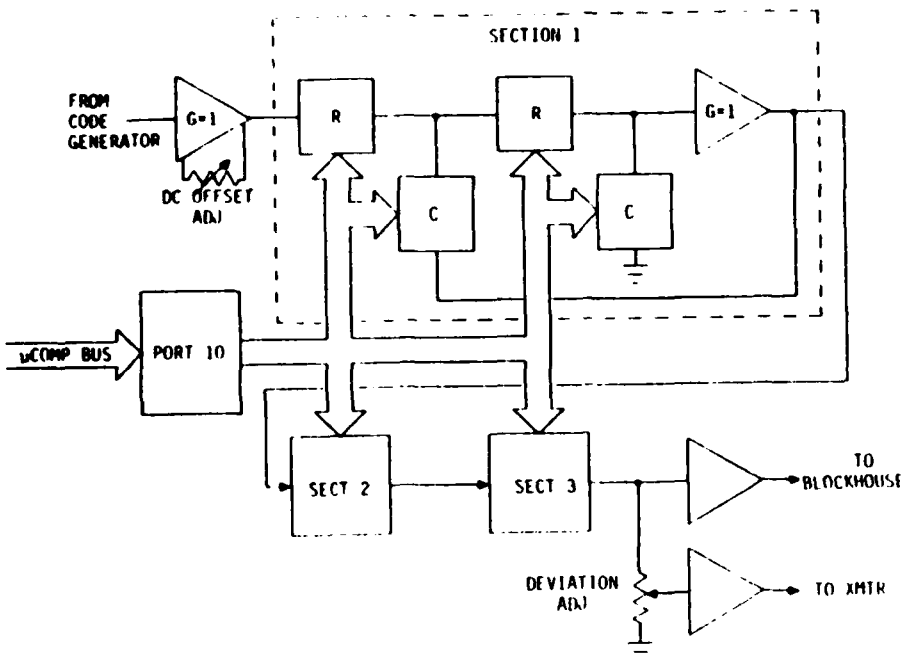

FIGURE 6. PREMODULATION FILTER AND OUTPUT DRIVES

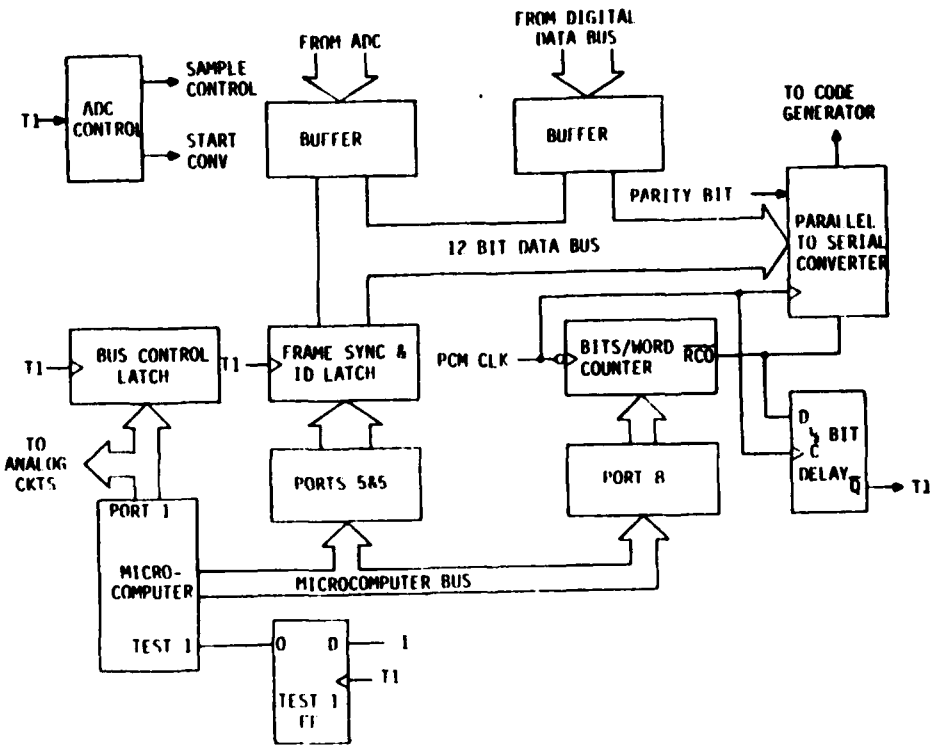

FIGURE 7. TIMING CIRCUIT BLOCK DIAGRAM

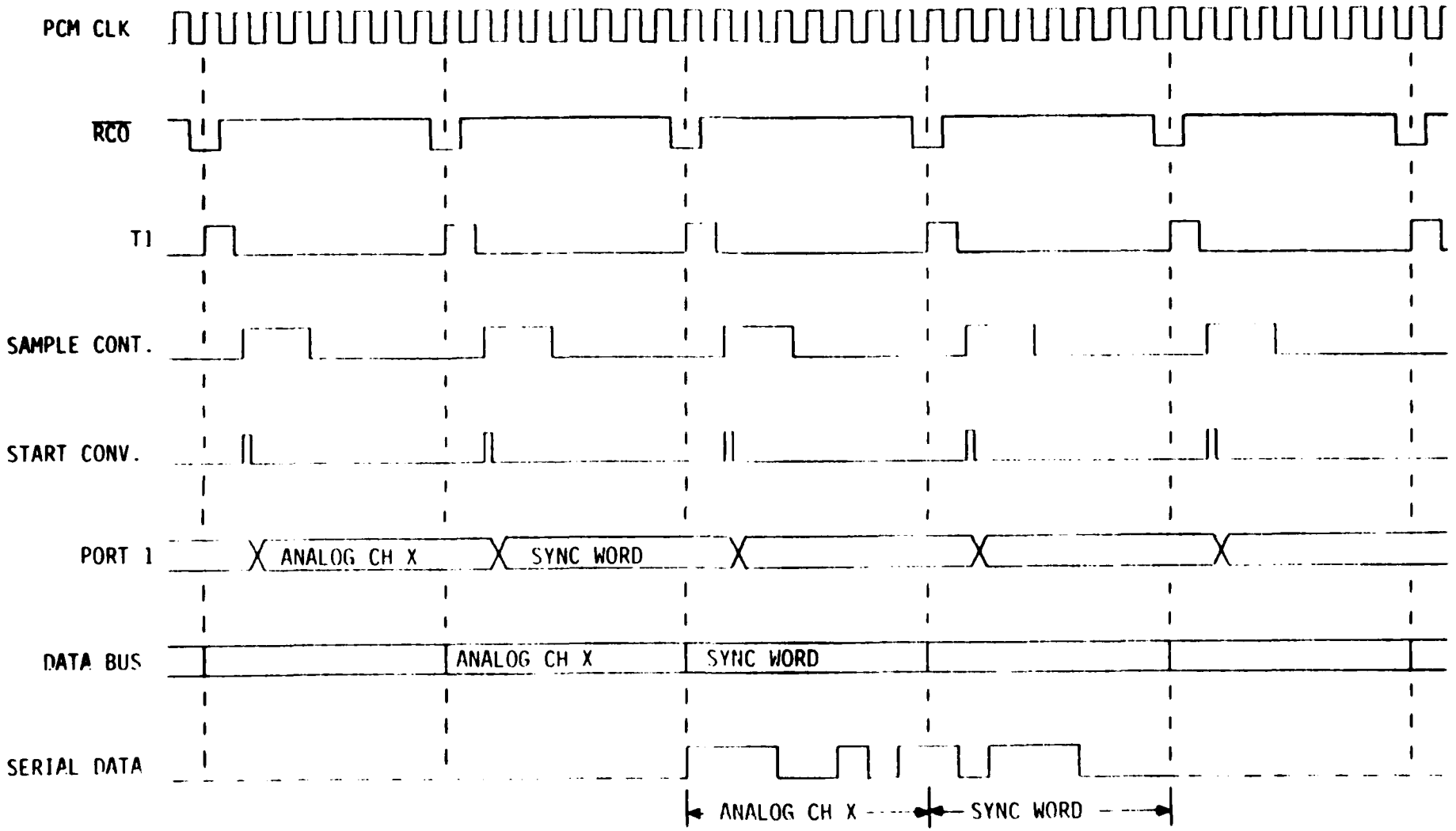

FIGURE 8. TIMING DIAGRAM

GLOSSARY OF TERMS

EPROM: An acronym for erasable programmable read only memory - A semiconductor integrated circuit into which digital information can be stored indefinitely without being powerd, but can be erased for reprogramming by exposure to ultraviolet light.

EEPROM: Same function as the EPROM above except that it is electrically erasable.

MICROCOMPUTER: (As used in this text) A single silicon chip integrated circuit containing a central processor, read only memory, random access memory, instruction decoder and input/output ports.

MULTIPLEXER: (MUX) An analog or digital device for selecting one of a number of inputs and switching this information to its output.

OUTPUT PCM CODES: A family of binary codes usually derived from a basic code where a "1" level is represented by a certain voltage or current level and a "0" level is represented by another. The different codes have characteristics which can improve transmission and recording, depending on the particular application. (See Reference 2)

PARITY: A system of error detection where an additional bit of information is added to each digital data word such as to make the number of "ones" either even or odd. This is done to verify the accuracy of transmission.

PULSE CODE MODULATION: (PCM) A process of data acquisition where analog signals are sequentially sampled and converted to a series of binary digits which represent the magnitude of the analog signal.

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